Delson
Technology Co, Ltd.

D916866G28NYJY
256M x 64 HIGH PERFORMANCE UNBUFFERED DDR2 SDRAM SODIMM

Features

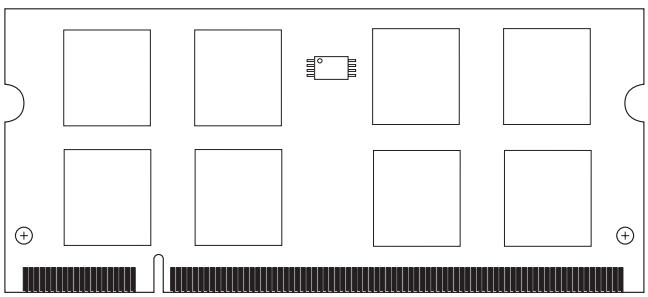
- 200-pin, unbuffered small outline, dual in-line memory module (SODIMM)
- JEDEC standard 1.8V ± 0.1V power supply
- VDDQ=1.8V ± 0.1V
- Fast data transfer rate: PC2-4200, PC2-5300, or PC2-6400
- Programmable CAS Latency(CL): 4, 5, 6
- Programmable Additive Latency(AL): 0, 1, 2, 3 4 and 5
- Write Latency(WL) = Read Latency (RL)-1
- Programmble burst lengths: 4 or 8
- Differential data strobe (DQS, DQS#) (Single ended data strobe option)
- On-die termination (ODT)
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- Serial Presence Detect (SPD) with EEPROM

Description

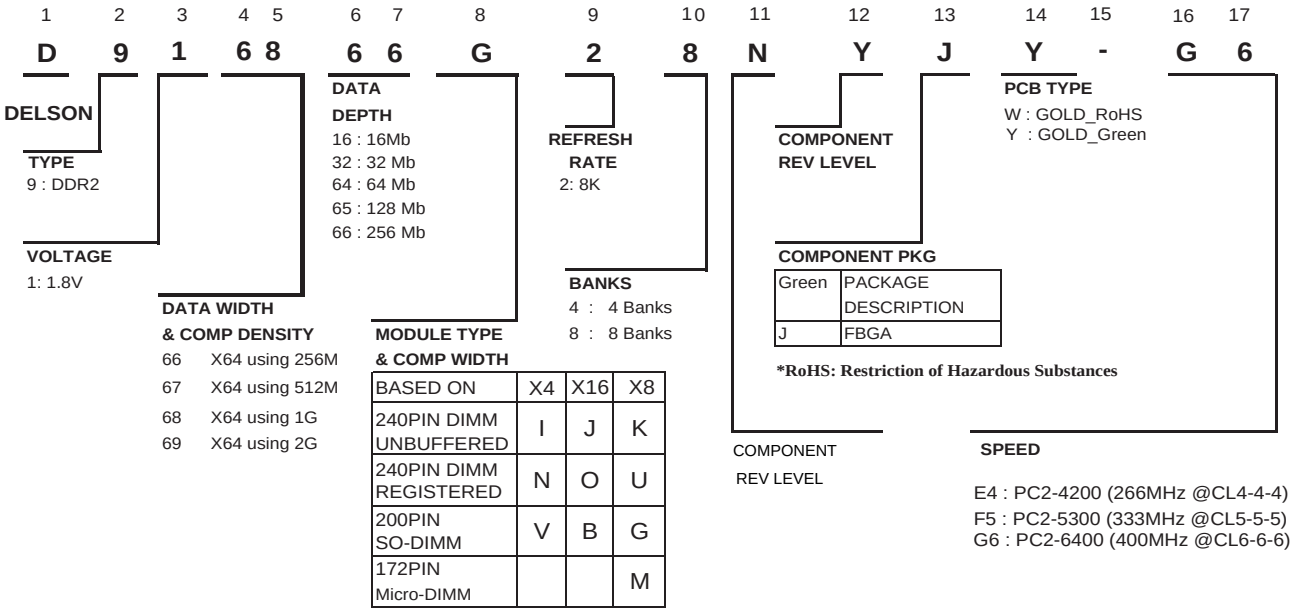
The D916866G28NYJY memory module is organized as 268,435,456 x 64 bits in a 200 pin memory module. The 256M x 64 memory module uses 16 DELSON 128M x 8 DDR2 SDRAMs. The x64 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

Speed Grade

	DDR2-533 PC2-4200 (E4)	DDR2-667 PC2-5300 (F5)	DDR2-800 PC2-6400 (G6)	Units
Bandwith@CL=4	533	533	533	Mbps
Bandwith@CL=5	533	667	667	Mbps
Bandwith@CL=6	533	667	800	Mbps
CL-tRCD-tRP	4-4-4	5-5-5	6-6-6	tCK

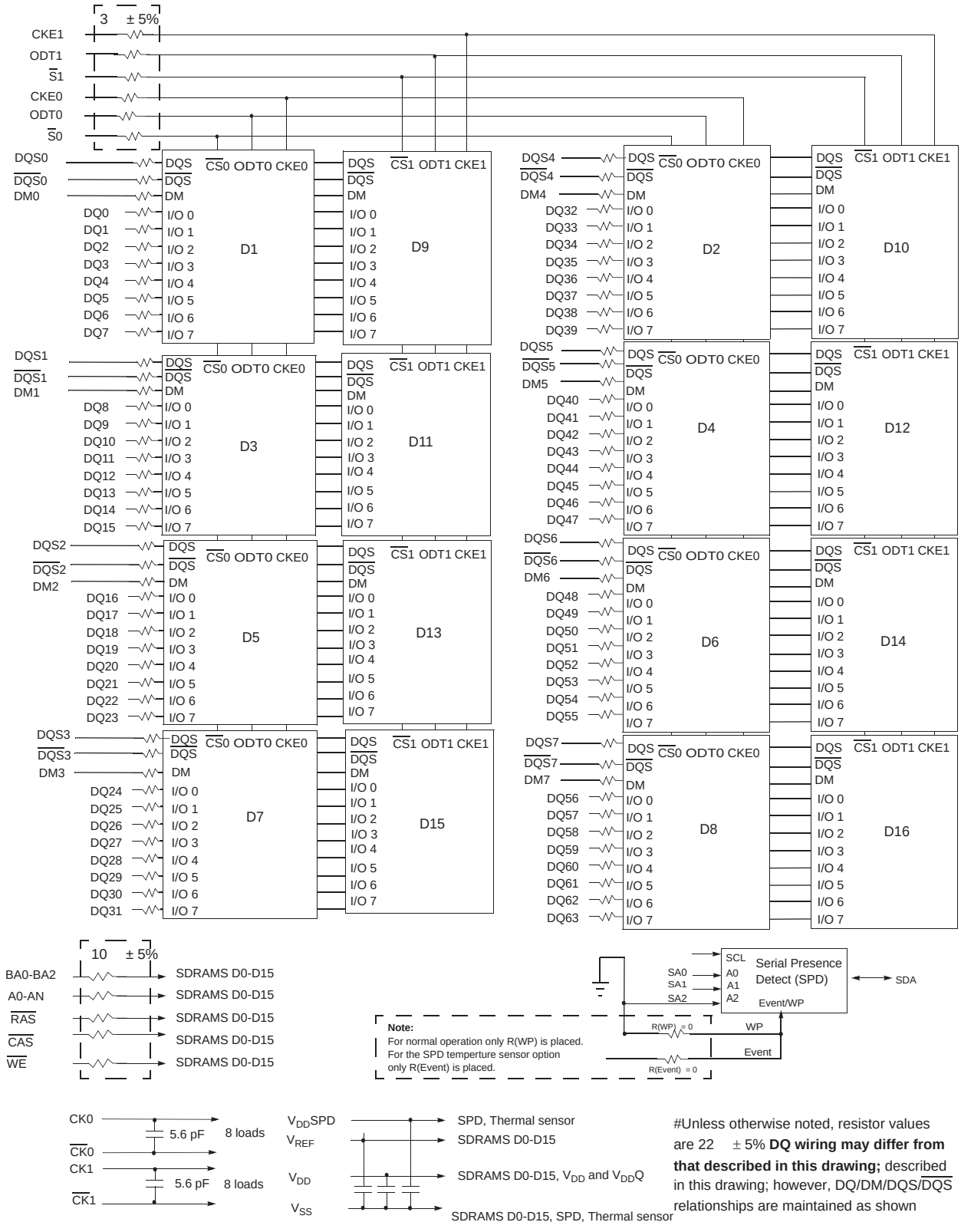


Part Number Information



BASED ON	X4	X16	X8
240PIN DIMM UNBUFFERED	I	J	K
240PIN DIMM REGISTERED	N	O	U
200PIN SO-DIMM	V	B	G
172PIN Micro-DIMM			M

Block Diagram:



#Unless otherwise noted, resistor values are 22 ± 5% **DQ wiring may differ from that described in this drawing;** described in this drawing; however, DQ/DM/DQS/$\overline{DQS}$ relationships are maintained as shown

DDR2 SDRAM SO-DIMM Pinout

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V_{REF}	2	V_{SS}	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	V_{SS}	4	DQ4	53	V_{SS}	54	V_{SS}	103	V_{DD}	104	V_{DD}	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	V_{SS}	156	V_{SS}
7	DQ1	8	V_{SS}	57	DQ19	58	DQ23	107	BA0	108	$\overline{RAS}$	157	DQ48	158	DQ52
9	V_{SS}	10	DM0	59	V_{SS}	60	V_{SS}	109	$\overline{WE}$	110	$\overline{S}0$	159	DQ49	160	DQ53
11	$\overline{DQS}0$	12	V_{SS}	61	DQ24	62	DQ28	111	V_{DD}	112	V_{DD}	161	V_{SS}	162	V_{SS}
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	$\overline{CAS}$	114	ODT0	163	NC,TEST	164	CK1
15	V_{SS}	16	DQ7	65	V_{SS}	66	V_{SS}	115	NC/ $\overline{S}1$	116	NC / A13	165	V_{SS}	166	$\overline{CK}1$
17	DQ2	18	V_{SS}	67	DM3	68	$\overline{DQS}3$	117	V_{DD}	118	V_{DD}	167	$\overline{DQS}6$	168	V_{SS}
19	DQ3	20	DQ12	69	**NC/$\overline{RE}$ $\overline{SET}$**	70	DQS3	119	NC / ODT1	120	**NC/$\overline{S}3$**	169	DQS6	170	DM6
21	V_{SS}	22	DQ13	71	V_{SS}	72	V_{SS}	121	V_{SS}	122	V_{SS}	171	V_{SS}	172	V_{SS}
23	DQ8	24	V_{SS}	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	V_{SS}	78	V_{SS}	127	V_{SS}	128	V_{SS}	177	V_{SS}	178	V_{SS}
29	$\overline{DQS}1$	30	CK0	79	CKE0	80	NC / CKE1	129	$\overline{DQS}4$	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	$\overline{CK}0$	81	V_{DD}	82	V_{DD}	131	DQS4	132	V_{SS}	181	DQ57	182	DQ61
33	V_{SS}	34	V_{SS}	83	**NC/$\overline{S}2$**	84	NC / A15	133	V_{SS}	134	DQ38	183	V_{SS}	184	V_{SS}
35	DQ10	36	DQ14	85	NC/BA2	86	NC / A14	135	DQ34	136	DQ39	185	DM7	186	$\overline{DQS}7$
37	DQ11	38	DQ15	87	V_{DD}	88	V_{DD}	137	DQ35	138	V_{SS}	187	V_{SS}	188	DQS7
39	V_{SS}	40	V_{SS}	89	A12	90	A11	139	V_{SS}	140	DQ44	189	DQ58	190	V_{SS}
41	V_{SS}	42	V_{SS}	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V_{SS}	193	V_{SS}	194	DQ63
45	DQ17	46	DQ21	95	V_{DD}	96	V_{DD}	145	V_{SS}	146	$\overline{DQS}5$	195	SDA	196	V_{SS}
47	V_{SS}	48	V_{SS}	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	$\overline{DQS}2$	50	$\overline{Event}$	99	A3	100	A2	149	V_{SS}	150	V_{SS}	199	V_{DD}SPD	200	SA1

Note:

1. NC = No Connect; NC,TEST(pin 163) is for bus analysis tool and is not connected on normal memory modules.
2. Pins 69, 83, 120 used by 4 rank DDR2 SO-DIMMs.

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0/$\overline{CK}$0, CK1/$\overline{CK}$1	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	Input	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S}$[1:0]	Input	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S}$0; Rank 1 is selected by $\overline{S}$1.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$ and $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA[2:0]	Input	—	Selects which DDR2 SDRAM internal bank of four or eight is activated.
ODT[1:0]	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR2 SDRAM mode register.
A[9:0], A10/AP, A[15:11]	Input	—	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ[63:0]	In/Out	—	Data Input/Output pins.
DM[7:0]	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS[7:0], $\overline{DQS}$[7:0]	In/Out	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
V_{DD}, V_{DD}SPD, V_{SS}	Supply	—	Power supplies for core, I/O, Serial Presence Detect, Thermal sensor, and ground for the module.
V_{REF}	Supply	—	Reference voltage for SSTL18 inputs.
SDA	In/Out	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM or Thermal sensor. A resistor must be connected from the SDA bus line to V_{DD}SPD on the system planar to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM and Thermal sensor.
SA[1:0]	Input	—	Address pins used to select the Serial Presence Detect base address.
TEST	In/Out	—	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (SO-DIMMs).
$\overline{Event}$	Wire-OR Out	Active Low	The optional EVENT pin is reserved for use to flag critical module temperatures and is used in conjuction with a SPD temperture sensing option.

Absolute Maximum DC Ratings

Parameter	Symbol	MIN	MAX	UNITS
VDD Supply Voltage relative to VSS	VDD	-1.0	2.3	V
VDDQ Supply Voltage relative to VSS	VDDQ	-0.5	2.3	V
VDDL Supply Voltage relative to VSS	VDDL	-0.5	2.3	V
Voltage on any pin relative to VSS	VIN, VOUT	-0.5	2.3	V
Storage Temperature	T_{STG}	-55	100	^{o}C

Note: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device.

AC & DC Operating Conditions
Recommended DC Operating Conditions

Parameter	Symbol	MIN	NOM	MAX	UNITS	Notes
VDD Supply Voltage relative to VSS	VDD	1.7	1.8	1.9	V	1
VDDQ Supply Voltage relative to VSS	VDDQ	1.7	1.8	1.9	V	4
VDDL Supply Voltage relative to VSS	VDDL	1.7	1.8	1.9	V	4
I/O Reference Voltage	VREF	0.49xVDDQ	0.50xVDDQ	0.51xVDDQ	V	2
I/O Termination Voltage(system)	VTT	VREF-0.04	VREF	VREF+0.04	V	3

Note:
1. VDD and VDDQ must track each other. VDDQ must be less than or equal to VDD.
2. VREF is expected to equal to VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak to Peak AC noise on the VREF may not exceed +/-2% VREF(DC).
3. VTT of the transmitting device must track VREF of receiving device.
4. VDDQ tracks with VDD; VDDL tracks with VDD.

Input Electrical Characteristics and operating Conditions

Input DC Logic Levels

Parameter	Symbol	MIN	MAX	UNITS
Input High (Logic 1) Voltage	VIH(DC)	VREF+0.125	VDDQ+0.3	V
Input Low (Logic 0) Voltage	VIL(DC)	-0.3	VREF-0.125	V

Input AC Logic Levels

Parameter	Symbol	MIN	MAX	UNITS
Input High (Logic 1) Voltage	VIH(AC)	VREF+0.200	-	V
Input Low (Logic 0) Voltage	VIL(AC)	-	VREF-0.200	V

DDR2 IDD Current Definitions

Symbol	Proposed Conditions		Units	Notes
IDD0	**Operating one bank active-precharge current**; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC (IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address businputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD2P	**Precharge power-down current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	
IDD2Q	**Precharge quiet standby current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputsare STABLE; Data bus inputs are FLOATING		mA	
IDD2N	**Precharge standby current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD3P	**Active power-down current**; All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	mA	
		Slow PDN Exit MRS(12) = 1mA	mA	
IDD3N	**Active standby current**; All banks open; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD5B	**Burst auto refresh current**; $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD6	**Self refresh current**; CK and CK\ at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	mA	
		Low Power	mA	
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $t_{RCD(IDD)}$-1*$t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$, $t_{RCD} = 1*t_{CK(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions		mA	

DDR2 IDD Current Table

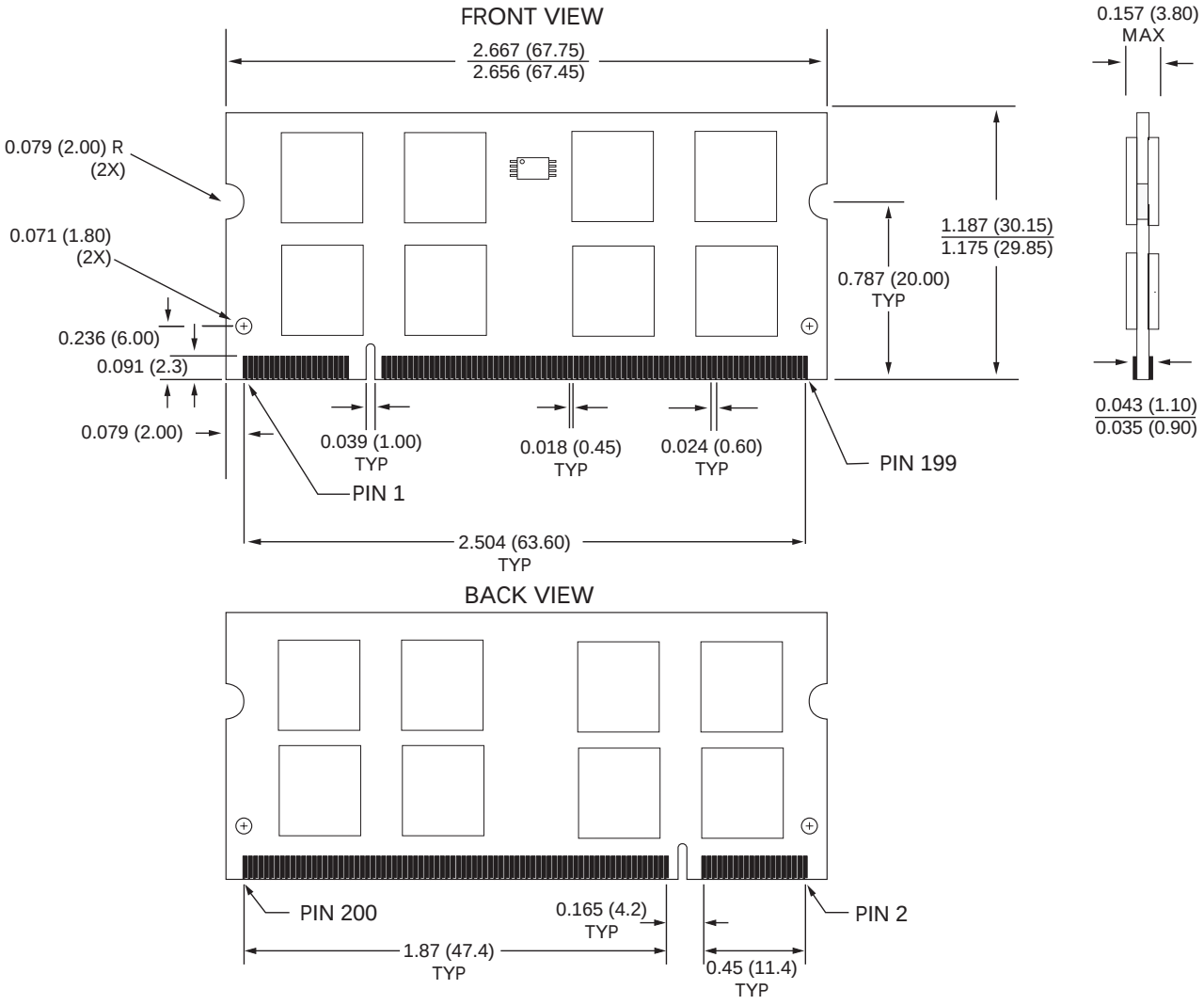
Symbol		E4 PC2-4200@CL4	F5 PC2-5300@CL5	G6 PC2-6400@CL6	Unit
IDD0		1184	1296	1400	mA
IDD1		1304	1416	1520	mA
IDD2P		240	240	240	mA
IDD2Q		640	720	800	mA
IDD2N		640	720	800	mA
IDD3P	Fast PDN Exit MR[12]=0	480	528	608	mA
	Slow PDN Exit MR[12]=1	288	288	288	mA
IDD3N		1088	1152	1200	mA
IDD4R		2064	2256	2520	mA
IDD4W		1920	2120	2400	mA
IDD5B		2400	2480	2560	mA
IDD6		128	128	128	mA
IDD7		2200	2440	2520	mA

AC Characteristics (AC operating conditions unless otherwise noted)

Parameter		Symbol	(DDR2-533) -37		(DDR2-667) -3		(DDR2-800) -25		Unit
			Min	Max	Min	Max	Min	Max	
Row Cycle Time		t_{RC}	60	-	60	-	57.5	-	ns
Auto Refresh Row Cycle Time		t_{RFC}	127.5	-	127.5	-	127.5	-	ns
Row Active Time		t_{RAS}	45	70K	45	70K	45	70K	ns
Row Address to Column Address Delay		t_{RCD}	15	-	15	-	12.5	-	ns
Row Active to Row Active Delay (x4 & x8)		t_{RRD}	7.5	-	7.5	-	7.5	-	ns
Row Active to Row Active Delay (x16)		t_{RRD}	10	-	10	-	10	-	ns
Column Address to Column Address Delay		t_{CCD}	2	-	2	-	2	-	CLK
Row Precharge Time		t_{RP}	15	-	15	-	12.5	-	ns
Write Recovery Time		t_{WR}	15	-	15	-	15	-	ns
Last Data-In to Read Command		t_{DRL}	1	-	1	-	1	-	CLK
Auto Precharge Write Recovery + Precharge Time		t_{DAL}	t_{WR} +t_{RP}	-	t_{WR} +t_{RP}	-	t_{WR} +t_{RP}	-	ns
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	t_{CK}	5	8	5	8	5	8	ns
	$\overline{CAS}$ Latency = 4		3.75	8	3.75	8	3.75	8	ns
	$\overline{CAS}$ Latency = 5		3.75	8	3	8	3	8	ns
	$\overline{CAS}$ Latency = 6		3.75	8	3	8	2.5	8	ns
Clock High Level Width		t_{CH}	0.45	0.55	0.48	0.52	0.48	0.52	CLK
Clock Low Level Width		t_{CL}	0.45	0.55	0.48	0.52	0.48	0.52	CLK
Data-Out edge to Clock edge Skew		t_{AC}	-0.50	0.50	-0.45	0.45	-0.40	0.40	ns
DQS-Out edge to Clock edge Skew		t_{DQSCK}	-0.45	0.45	-0.40	0.40	-0.35	0.35	ns
DQS-Out edge to Data-Out edge Skew		t_{DQSQ}	-	0.30	-	0.24	-	0.20	ns
Data-Out hold time from DQS		t_{QH}	t_{HPmin} -t_{QHS}	-	t_{HPmin} -t_{QHS}	-	t_{HPmin} -t_{QHS}	-	ns
Data hold skew factor		t_{QHS}	-	400	-	340	-	300	ps
Clock Half Period		t_{HP}	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	ns
Input Setup Time (fast slew rate)		t_{IS}	250	-	200	-	175	-	ps
Input Hold Time (fast slew rate)		t_{IH}	375	-	275	-	250	-	ps
Input Pulse Width		t_{IPW}	0.35	-	0.60	-	0.60	-	CLK
Write DQS High Level Width		t_{DQSH}	0.35		0.35		0.35		CLK
Write DQS Low Level Width		t_{DQSL}	0.35		0.35		0.35		CLK
CLK to First Rising edge of DQS-In		t_{DQSS}	WL- 0.25t_{CK}	WL+ 0.25t_{CK}	WL- 0.25t_{CK}	WL+ 0.25t_{CK}	WL- 0.25t_{CK}	WL+ 0.25t_{CK}	CLK
Data-In Setup Time to DQS-In (DQ & DM)		t_{DS}	100	-	100	-	50	-	ps
Data-in Hold Time to DQS-In (DQ & DM)		t_{DH}	175	-	175	-	125	-	ps
DQS falling edge to CLK rising Setup Time		t_{DSS}	0.2	-	0.2	-	0.2	-	CLK

Parameter	Symbol	(DDR2-533) -37		(DDR2-667) -3		(DDR2-800) -25		Unit
		Min	Max	Min	Max	Min	Max	
DQS falling edge from CLK rising Hold Time	t_{DSH}	0.2	-	0.2	-	0.2	-	CLK
DQ & DM Input Pulse Width	t_{DIPW}	0.35	-	0.35	-	0.35	-	CLK
Read DQS Preamble Time	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	CLK
Read DQS Postamble Time	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	CLK
Write DQS Preamble Setup Time	t_{WPRES}	0	-	0	-	0	-	CLK
Write DQS Preamble Hold Time	t_{WPREH}	0.25	-	0.25	-	0.25	-	CLK
Write DQS Postamble Time	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	CLK
Internal read to precharge command delay	t_{RTP}	7.5	-	7.5	-	7.5	-	ns
Internal write to read command delay	t_{WTR}	7.5	-	7.5	-	7.5	-	ns
Data out high impedance time from CLK/$\overline{CLK}$	t_{HZ}	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	ns
Data out low impedance time from CLK/$\overline{CLK}$	t_{LZ}	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	ns
Mode Register Set Delay	t_{MRD}	2	-	2	-	2	-	CLK
Exit Self Refresh to Non-Read Command	t_{XSNR}	t_{RFC}+10	-	t_{RFC}+10	-	t_{RFC}+10	-	ns
Exit Self Refresh to Read Command	t_{XSRD}	200	-	200	-	200	-	CLK
Exit Precharge Power Down to any non-Read Command	t_{XP}	2	-	2	-	2	-	CLK
Exit Active Power Down to Read Command	t_{XARD}	2	-	2	-	2	-	CLK
Exit Active Power Down to Read Command (Slow exit, Lower Power)	t_{XARDS}	6-AL	-	7-AL	-	8-AL	-	CLK
ODT drive mode output delay	t_{OIT}	0	12	0	12	0	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	t_{Delay}	tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		ns
CKE minimum high and low pulse width	t_{CKE}	3	-	3	-	3	-	CLK

Package Dimension



NOTE:

All dimensions are in inches (millimeters); $\frac{MAX}{MIN}$ or typical where noted.

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